10016448 CLS

Most Frequently Occurring Classifications of Patents Returned From A Search of 10016448 on March 24, 2004

9 326/41 2 326/39 2 365/49 2. 438/129 2 714/724 2 716/16 Cross-Reference Classifications 11 326/39 5 326/38 4 326/41 3 326/47 2 326/37 2 438/599 2 439/189 2 710/8 2 714/733 2 714/734 2 716/17 2 716/4 2 716/7 Combined Classifications 13 326/39 13 326/41 5 326/38 3 326/37 3 326/47 3 716/16 3 716/17 2 326/40 2 365/49 2 376/216 2 438/129 2 438/599 2 439/189 2 703/15 2 703/23 2 703/25 2 703/28 2 710/100 2 710/8 2 713/400

Original Classifications

10016448_CLS

- 714/33
- 714/724 714/733
- 714/734

- 2 2 2 2 2 2 716/18 716/4 716/7

 ${\tt 10016448_CLSTITLES}\\ {\tt Titles\ of\ Most\ Frequently\ Occurring\ Classifications\ of\ Patents\ Returne}$

From A Search of 10016448 on March 24, 2004

13	326/39 Class 326/37 326/39	(2 OR, 11 XR) 326: ELECTRONIC DIGITAL LOGIC CIRCUITRY MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.) .Array (e.g., PLA, PAL, PLD, etc.)
13	326/41 Class 326/37 326/39 326/41	UNIVERSAL, ETC.)
5		(0 OR, 5 XR) 326: ELECTRONIC DIGITAL LOGIC CIRCUITRY MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.) .Having details of setting or programming of interconnections or logic functions
3		(1 OR, 2 XR) 326: ELECTRONIC DIGITAL LOGIC CIRCUITRY MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.)
3		(0 OR, 3 XR) 326: ELECTRONIC DIGITAL LOGIC CIRCUITRY MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.) .Significant integrated structure, layout, or layout interconnections
3	716/16 Class 716/1 716/12 716/16	
3	716/17 Class	(1 OR, 2 XR) 716: DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK

	716/1 716/17		10016448_CLSTITLES CIRCUIT DESIGN .Programmable integrated circuit (e.g., basic cell, standard cell, macrocell)
2	326/40 Class 326/37	326	OR, 1 XR) : ELECTRONIC DIGITAL LOGIC CIRCUITRY MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.) .Array (e.g., PLA, PAL, PLD, etc.)
	326/40		With flip-flop or sequential device
2		365	OR, 0 XR) : STATIC INFORMATION STORAGE AND RETRIEVAL ASSOCIATIVE MEMORIES
2	376/216 Class 376/207	376	: INDUCED NUCLEAR REACTIONS: PROCESSES, SYSTEMS, AND ELEMENTS
			COOLANT FLOW)
	376/215		<pre>.By electronic signal processing circuitry (e.g., plural redundant circuits)</pre>
	376/216		Plural sensed different conditions or measured variables correlated
2	438/129 Class		OR, 0 XR) : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS
	438/128		MAKING DEVICE ARRAY AND SELECTIVELY INTERCONNECTING
	438/129		
2	438/599 Class		OR, 2 XR) : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS
	438/584		COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
	438/597		.To form ohmic contact to semiconductive material
	438/598		Selectively interconnecting (e.g., customization, wafer scale integration, et
c.)	438/599		With electrical circuit layout
2	439/189 Class 439/189	439	OR, 2 XR) : ELECTRICAL CONNECTORS WITH OR COMPRISING REMOVABLE CIRCUIT MODIFYING ARRANGEMENT

10016448_CLSTITLES

			•••
2	703/15 Class 703/13 703/14 703/15	703	OR, 1 XR) : DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION SIMULATING ELECTRONIC DEVICE OR ELECTRICAL SYSTEM .Circuit simulationIncluding logic
2	703/23 Class 703/23	703	OR, 1 XR) : DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION EMULATION
2		703	OR, 1 XR) : DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION EMULATION .Of peripheral deviceI/O adapter (e.g., port, controller)
2	703/23	703	OR, 1 XR) : DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION EMULATION .In-circuit emulator (i.e., ICE)
2		710	OR, 1 XR) : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
2	710/8 Class 710/1 710/8	710	OR, 2 XR) : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT INPUT/OUTPUT DATA PROCESSING .Peripheral configuration
2	713/400 Class 713/400	713	OR, 1 XR) : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: SUPPORT SYNCHRONIZATION OF CLOCK OR TIMING SIGNALS, DATA, OR PULSES
2	714/33 Class		OR, 1 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY

Page 3

	714/100		10016448_CLSTITLES DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING
	714/1 714/25		<pre>.Reliability and availabilityFault locating (i.e., diagnosis or testing)</pre>
	714/32 714/33		<pre>Particular stimulus creationDerived from analysis (e.g., of a specification or by stimulation)</pre>
2	714/724 Class		OR, 0 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
	714/699 714/724		PULSE OR DATA ERROR HANDLING Digital logic testing
2	714/733 Class		: ERROR DETECTION/CORRECTION AND FAULT
	714/699 714/724 714/733		DETECTION/RECOVERY PULSE OR DATA ERROR HANDLING .Digital logic testingBuilt-in testing circuit (BILBO)
2		(0 714	OR, 2 XR) : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
	714/699 714/724 714/734		
2			OR, 1 XR) : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1 716/18		CIRCUIT DESIGN .Logical circuit synthesizer
2	716/4 Class		OR, 2 XR) : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1 716/4		CIRCUIT DESIGN .Testing or evaluating
2	716/7 Class		, 2 XR) DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1 716/7		CIRCUIT DESIGN .Partitioning (e.g., function block, ordering constraint)

10016448_LIST PLUS Search Results for S/N 10016448, Searched March 24, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated sear ch

system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that a re

most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

10016448_LIST

5910725 5959489
5959489
05.,,52
6147890
6211697
6211697
6297666
6301696
6331790
6334169
6476636
6504398
6531891

10016448 QUAL

6476636 72

5841790 90

Page 1

10016448_QUAL

6504398 72 6531891 72